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Three-Phase Seventeen-Level Cascaded Switched-Capacitor Multilevel Inverter for Grid-Connected PV Systems

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Abstract: The topology of grid-connected three-phase 17-level Cascaded Switched Capacitor Multilevel Inverter (CSC-MLI) for photovoltaic systems (PV) is proposed in this work. Each phase of the proposed inverter is formed by cascading two identical 9-level SC-MLI basic cells, resulting in a 17-level CSC-MLI configuration to comply with IEEE standards for minimal Total Harmonic Distortion (THD) in grid-tied inverters. The proposed inverter has the feature of self-balancing capacitor voltage ability, self-boosting voltage capability, and limiting the capacitor inrush current during the capacitor charging mode, in addition, the ability of reactive power support. A new hybrid pulse width modulation (PWM) has been implemented with a 2.5 kHz frequency to produce the gate pulses. The proposed three-phase CSC-MLI is connected to a multi-array PV system through a single DC bus bar collector to enable an inherently balanced power share between the CSC-MLI cells and phases. The simulation results show that the proposed inverter achieves a THD of less than 1% in its output current. The MATLAB/Simulink software was employed to simulate the steady-state and dynamic performance of the proposed 12 kW PV grid-connected three-phase CSC-MLI under a variety of environmental conditions and power factors.

Keywords: Multilevel inverter, Cascaded switched-capacitor, Hybrid-pulse width modulation, Total harmonic distortion (THD), Renewable energy.

Introduction

In the growth of sustainable and reliable power systems, Multilevel inverters (MLIs) are the most popular and advanced technology for power conversion systems, which are essential for a variety of applications, including photovoltaic, devices, wind turbines, and so on (Ali, 2022; Barzegarkhoo, 2017). MLIs possess several advantageous characteristics that distinguish them from traditional two-level inverters, such as reduced THD, lower blocking voltage ratings, reduced voltage derivatives (dv/dt) stress, and reduced output filter size (Akagi, 2017;Hassan, 2020; Panda et al., 2019). In general, MLIs are categorized into three topologies: cascaded H-bridge (CHB), neutral-point clamped (NPC), and floating capacitor (FC). Besides providing suitable performance, each of these three conventional topologies has its own set of constraints, including the requirement for numerous isolated DC sources in the CHB topology and the capacitor voltage imbalance in the NPC and FC topologies (Bana, 2019; Saccol, 2018). Additionally, a large number of components is required for conventional MLIs while producing more level of output voltage and face challenges related to switching losses and higher stress on switches, which increases cost, reduces efficiency, and thus creates a hindrance to providing better performance for modern power systems (Omer, 2020; Hassan et al.,2024).

Switched-capacitor multi-level inverters (SC-MLIs) are novel topologies that serve as an efficient and enhanced substitute to typical MLIs for conquering the drawbacks of existing designs (Kumari, 2021). The recent SC-MLIs

emerged as a fundamental basis for producing the greatest voltage levels with the lowest possible THD content while minimizing the count of input DC sources and switches and reducing the voltage stress on switches. In addition, SC-MLIs have a feature of inherent capacitor voltage balancing capability without employing extra circuits or sophisticated control techniques, easing the control complexity of circuits (Deng et al., 2023). In this line, the author in Babaei and Gowgani (201) suggests a topology that aims to minimize the circuit complexity by decreasing the number of switches and the requirement for isolated DC sources by connecting the capacitors in series or parallel with the input DC source. Recent efforts have focused on developing SC-MLIs capable of higher voltage levels to produce high-quality sinusoidal output voltage waveforms with minimal components. In Dhanamjayulu et al. (2021), the authors proposed a 17-level hybrid CHB with a minimal switch count, comprising 14 switches, 4 input DC sources, and 4 capacitors, which effectively mitigates the CHB-related issues. Asymmetrical MLIs have been proposed to generate 13 voltage levels with the feature of inherent voltage polarity reversal capability using 14 power switches, two capacitors, and two unequal input DC sources (Samadei et al., 2018). Despite the effective utilization of capacitors in (Ghodsi & Barakati, 2019, 2020; Taghvaie et al., 2017), the number of switches remains high, with voltage stress equivalent to the boosting gain of the inverter. To mitigate the previous drawbacks, a new 13L SCMLI has been developed with fewer power switches in (Sandeep, 2020), including a boosting factor of 6 while constraining the maximum voltage stress across the switches to three times the input source. The inverter in Siddique et al. (2020) requires twenty-six switches, seven capacitors, and a DC supply, lowering inverter efficiency, increasing costs, and complicating system design. It employs a selective harmonic elimination PWM (SHE-PWM) strategy to lessen the impact of dominant harmonics. A 13-level SC-MLI with a boosting factor of 6 is introduced in Hussan et al. (2023). This design incorporates self-balancing capacitors voltage without auxiliary circuits and produces negative voltage levels without using an H-bridge. Additionally, Nearest Level Modulation scheme is used to improve the quality of the output voltage. Hussan et al. (2021) presents a new SC inverter using a reduced number of switches to generate a 15-level output voltage with a gain of 7 by using two input DC sources. The topology in Ali et al. (2018) yields a 17-level output with four asymmetrical DC sources. The combination of components enables higher voltage gain and more accurate control over output levels. This innovative design allows for versatility in power conversion applications while remaining efficient. This MLI architecture has a power mismatch problem, making it less viable. In the structures that have been previously presented, no solution has been proposed to restrict the capacitor inrush current, which represents one of the limitations of SC-MLIs structures during the capacitor charging process, where a significant inrush current increases the current stress on the switches involved in the charging path, making the converters less efficiency (Ali et al., 2022). Some methods have been developed to address the challenge of minimizing the capacitor spike current of SC-MLIs, including the soft charging method. The 17-level structure presented in Anand et al. (2023) uses the soft charging method to limit the capacitor spike current. Marangalu et al. (2023) proposed another 17-level modified inverter that can reduce the capacitor spike current by using two inductors along with freewheeling diodes. In Jahan et al. (2018), a 9-level topology with features of eliminating leakage current, input voltage boosting, and suitability for PV applications has been introduced. In this topology, an inductor is connected in series with the input DC source and charging switches to eliminate the high inrush current.

In this paper, the pre-existing single-phase 9-level MLI Baksi (2023) was successfully developed to propose a grid-connected three-phase 17-level cascaded switched-capacitor multilevel inverter integrated with the PV systems through a single DC bus bar collector in such a way that eliminates the inherent unbalanced power supplied to the three-phase system when the PV array suffers from non-uniform irradiation or partial shading. The primary objectives of the proposed structure are producing 17- level output voltage waveform with lower THD by using a minimum count of components as compared to conventional MLIs, achieving self-balancing capacitor voltages without using auxiliary circuits, a self-voltage boosting ability, reducing the capacitor inrush current, Inherent polarity reversal capability, minimize the grid filter requirements, and achieving suitable values for Total Standing Voltage (TSV).

This paper is organized as: The configuration description, operating states, PWM technique, and theoretical analysis of the proposed topology are described in Section 2. The control scheme of the proposed system is presented in Section 3. The comparison study is drawn in section 4. The results and discussion of the proposed inverter are explained in Section 5. Finally, the conclusion in Section 6.

Proposed Three-Phase 17-Level CSC-MLI Topology

Proposed Configuration Description

The grid-connected three-phase 17-level cascaded switched-capacitor multilevel inverter integrated with multi-array photovoltaic systems through a single DC Bus bar collector is illustrated in Fig. 1. The 17-level CSC-MLI

is constructed by cascading two identical 9-level basic cells. Each phase of the proposed structure comprises twelve unidirectional switches, six bi-directional switches, four diodes, four DC-link capacitors ($C_{11}, C_{12}, C_{21}, C_{22}$), four floating capacitors ($C_{13}, C_{14}, C_{23}, C_{24}$) and two soft charging inductors (L_{CH_1}, L_{CH_2}) along with freewheeling diodes (D_{f_1}, D_{f_2}) to minimize the capacitor inrush current. Two isolated DC sources for each phase with identical values are generated by the Flyback converter to supply each cell of the proposed inverter with DC-link voltage V_{dc}. The input DC-link voltage is evenly distributed across the DC-link capacitor string. Therefore, the voltage across each of them is equal to ($V_{dc}/2$). The voltage across the floating capacitors string is equal to ($V_{dc}/4$) as they are charged to a voltage magnitude of ($V_{dc}/2$) and it remains in balance during the operating states.

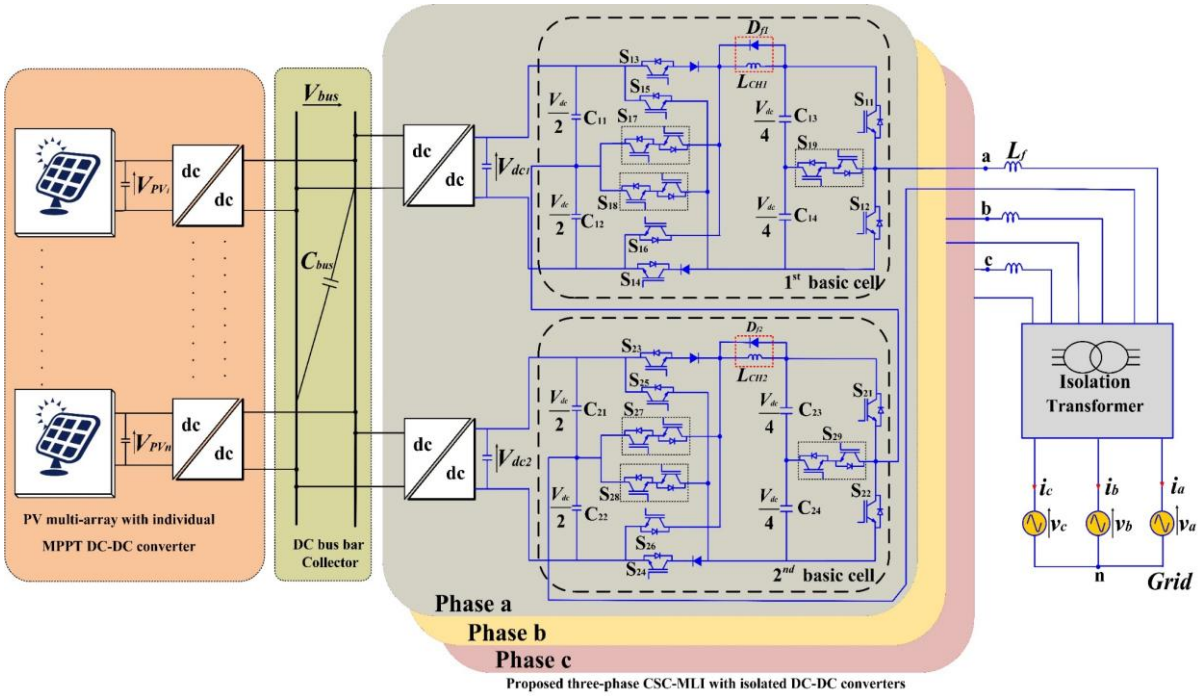


Figure 1. Grid-connected three-phase 17- Level CSC-MLI with PV multi-array single DC bus bar collector.

The proposed three-phase CSC-MLI is connected to the grid through an isolation transformer with a 1:1 turns ratio, which provides galvanic isolation between the inverter and grid for safety and to isolate each phase of the proposed inverter from each other. On the other hand, the suggested configuration illustrated in Fig. 1 comprises a multi-array PV system linked to a common DC bus bar using independent boost converters performing MPPT for each PV array to increase the energy conversion efficiency. The feature of this structure is to eliminate the per-cell and per-phase power unbalance issues in the three-phase systems when the PV arrays suffer from partial shading or non-uniform irradiation by concentrating the whole generated PV power in a common DC bus bar (Hassan, 2020). The DC bus is then connected to the three-phase CSC-MLI by using an isolated DC-DC flyback converter with a transformer of 1:1 turns ratio to ensure an inherently balanced power distribution between the CSC-MLI cells.

Operating Principle

As each phase of the proposed three-phase CSC-MLI consists of two identical 9-level MLI basic cells connected in series as cascade connection to produce 17 output voltage levels, the operating states of the 9-level basic cell will be explained in Fig. 2 according to the switching states of MLI based 9-level basic cell listed in Table 1.

Operating State 1 ($v_o = +0$): In this operation state, only the switches S_2, S_3, and S_8 are turned on. The load current flows through the path C_1-S_3-L_{CH}-C_3-C_4-S_2-C_1 as represented by the red line in Fig. 2 (a). The voltage across the floating capacitors string C_3 and C_4 is equal to ($V_{dc}/4$) as they charged to a voltage magnitude of ($V_{dc}/2$) from the DC-link capacitors through the switches S_3 and S_8 as indicated by a green dotted line and the voltage across them remains in balance during the operating states.

Table 1. Switching states of 9-level MLI basic cell

Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	Output voltage	V_{C_3}	V_{C_4}
1	0	1	1	0	0	0	0	1	0	$V_{C_1} - V_{C_3} - V_{C_4} = +0\ V_{dc}$	C	C
2	0	0	1	0	0	0	0	1	1	$V_{C_1} - V_{C_3} = +0.25\ V_{dc}$	C	C
3	1	0	1	0	0	0	0	1	0	$V_{C_1} = +0.5\ V_{dc}$	C	C
4	0	0	0	0	1	0	0	0	1	$V_{C_1} + V_{C_4} = +0.75\ V_{dc}$	NC	D
5	1	0	0	0	1	0	0	0	0	$V_{C_1} + V_{C_3} + V_{C_4} = +V_{dc}$	D	D
6	1	0	0	1	0	0	1	0	0	$V_{C_3} + V_{C_4} - V_{C_2} = -0\ V_{dc}$	C	C
7	0	0	0	1	0	0	1	0	1	$V_{C_4} - V_{C_2} = -0.25\ V_{dc}$	C	C
8	0	1	0	1	0	0	1	0	0	$-V_{C_2} = -0.5\ V_{dc}$	C	C
9	0	0	0	0	0	1	0	0	1	$-V_{C_3} - V_{C_2} = -0.75\ V_{dc}$	D	NC
10	0	1	0	0	0	1	0	0	0	$-V_{C_4} - V_{C_3} - V_{C_2} = -V_{dc}$	D	D

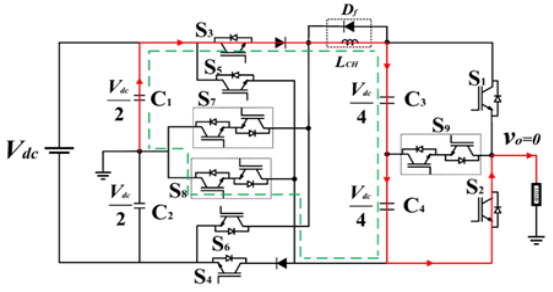
C= charging; D= discharging; NC= not change

Operating State 2 ($v_o = +0.25\ V_{dc}$): In this operation state, only S_3, S_8, and S_9 are in the ON state. The load current flows through the path C_1-S_3-L_{CH}-C_3-S_9-C_1 as donated by the red line in Fig. 2 (b). The floating capacitor string C_3 and C_4 charged to a voltage magnitude of $(V_{dc}/2)$ from the DC-link capacitor through the switches S_3 and S_8 as donated by a green dotted line.

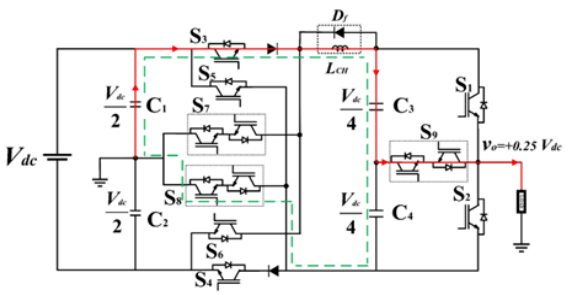
Operating State 3 ($v_o = +0.5\ V_{dc}$): In this operation state, only S_1, S_3, and S_8 are turned on. The load current flows through the path C_1-S_3-L_{CH}-S_1-C_1 as donated by the red line in Fig. 2 (c). The C_3 and C_4 charged to a voltage magnitude of $(V_{dc}/2)$ through the switches S_3 and S_8 as donated by a green dotted line.

Operating State 4 ($v_o = +0.75\ V_{dc}$): In this operation state, only S_5 and S_9 are in ON state. The load current flows through the path C_1-S_5-C_4-S_9-C_1 as donated by the red line in Fig. 2 (d). The capacitor C_4 is discharged through the load while C_3 is not charged or discharged.

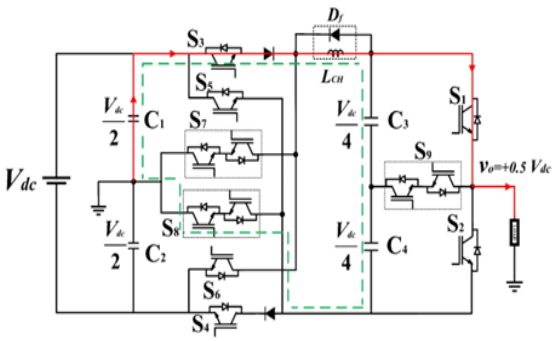
Operating State 5 ($v_o = +V_{dc}$): In this operation state, only S_1 and S_5 are turned on. The load current flows through the path C_1-S_5-C_4-C_3-S_1-C_1 as donated by the red line in Fig. 2 (e). The capacitors C_3 and C_4 are discharged through the load. The analysis for the remaining states, as depicted in Fig. 2 (f-j), is the same as the previously described operating states.



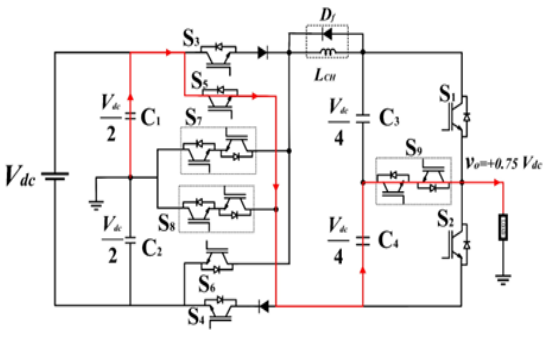
(a) Operating State 1



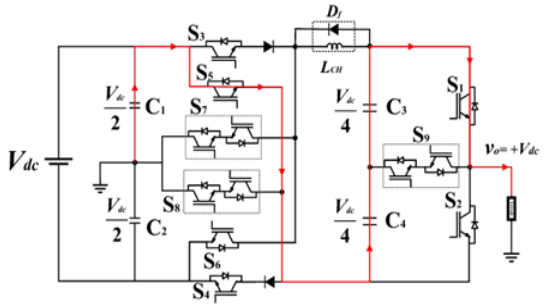
(b) Operating State 2



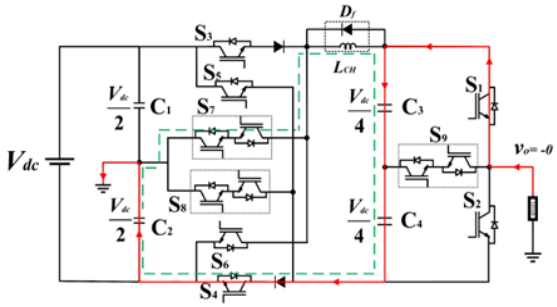
(c) Operating State 3



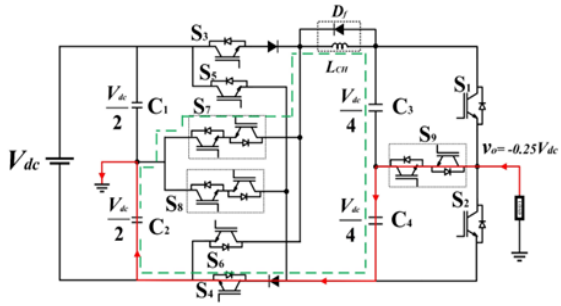
(d) Operating State 4



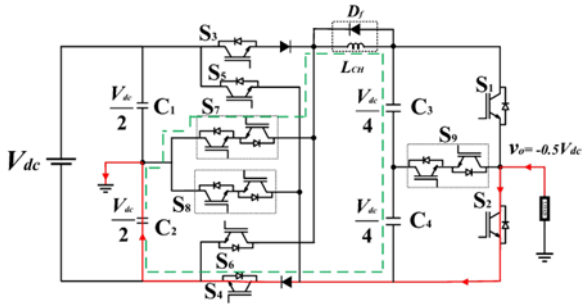
(e) Operating State 5



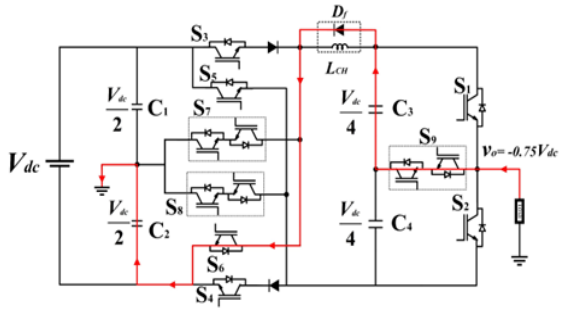
(f) Operating State 6



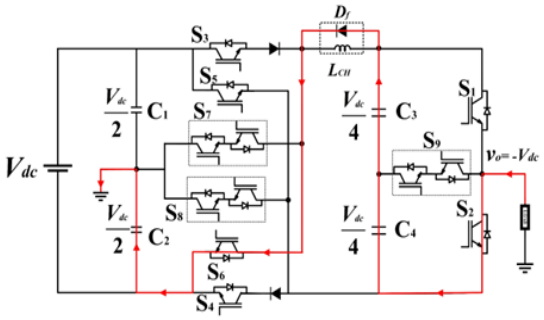
(g) Operating State 7



(h) Operating State 8



(i) Operating State 9



(j) Operating State 10

Figure. 2. Operation states of the 9-level MLI basic cell

PWM of Proposed Three-Phase 17-Level CSC-MLI

A variety of modulation strategies have been proposed for controlling multilevel inverters, including sinusoidal pulse width modulation (SPWM) (Sandeep, 2020), selective harmonic elimination (SHE) (Siddique et al., 2020), and nearest level control (NLC) (Hussan et al., 2023), to minimize the operational complexity and generates an output waveform with lower THD, a Hybrid-PWM has been proposed, which is a combination between the Level Shifted-PWM (LS-PWM) and Phase Shifted-PWM (PS-PWM) to generate the drive signal of the switches for producing a 17-level waveform for each phase of the proposed inverter according to the logic circuit given in Fig.3.

Three-phase sinusoidal reference signals ($V_{ref\_a}, V_{ref\_b}, V_{ref\_c}$) with reversed negative half cycle have been compared with four level shifted carrier signals ($V_{Cr_{11}}, V_{Cr_{12}}, V_{Cr_{13}}, V_{Cr_{14}}$) to produce the gate pulses of the first basic cell in each phase. Similarly, four phase shifted triangular carrier signals ($V_{Cr_{21}}, V_{Cr_{22}}, V_{Cr_{23}}, V_{Cr_{24}}$),whose out of phase with the level shifted carrier signals are used to generate the second basic cell's gating pulses by comparing them with the reference signals, as seen in Figure 4. The feature of the reversed negative half cycle is to minimize the carrier signals from 16 to 8 as compared with the non-reversed one. Each carrier signal has same amplitude and a 2.5 kHz frequency. The suggested Hybrid-PWM modulation index is denoted as:

$$m_a = \frac{\hat{V}_{ref\_x}}{4\hat{V}_{Cr}} \qquad 0 \le m_a \le 1 \tag{1}$$

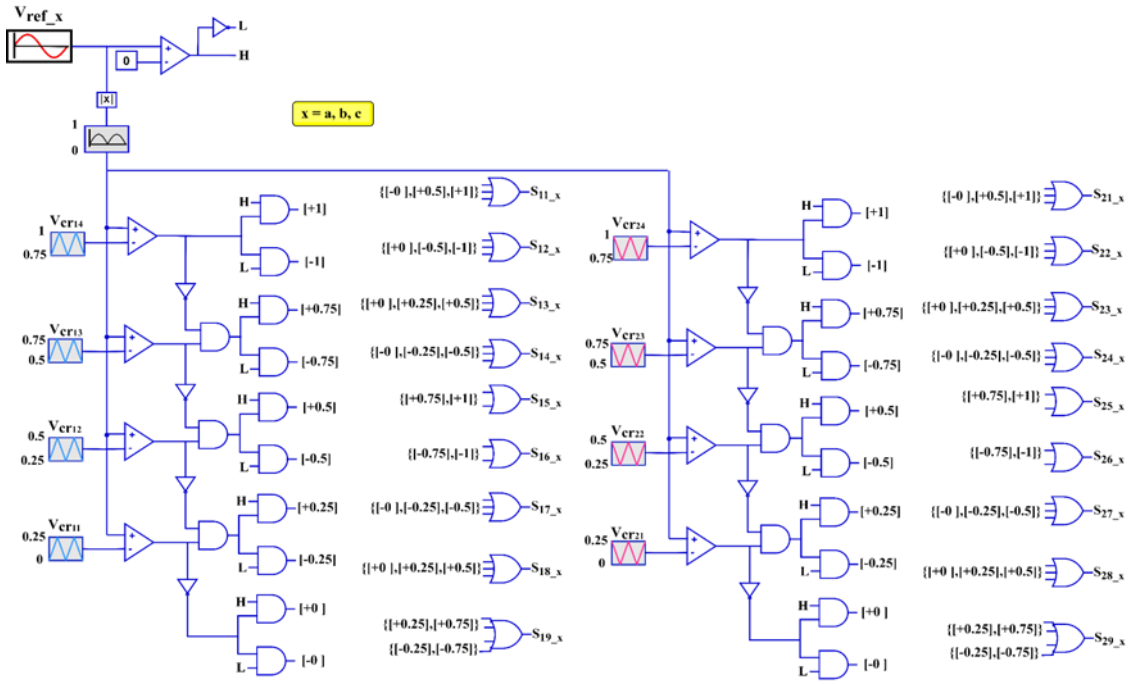


Figure 3. Modulation logic of the proposed three-phase CSC-MLI

where m_a represents the amplitude modulating index, $\hat{V}_{ref\_x}$ and $\hat{V}_{Cr}$ are the peak value of the reference and each carrier signal, respectively where x is a, b and c phas

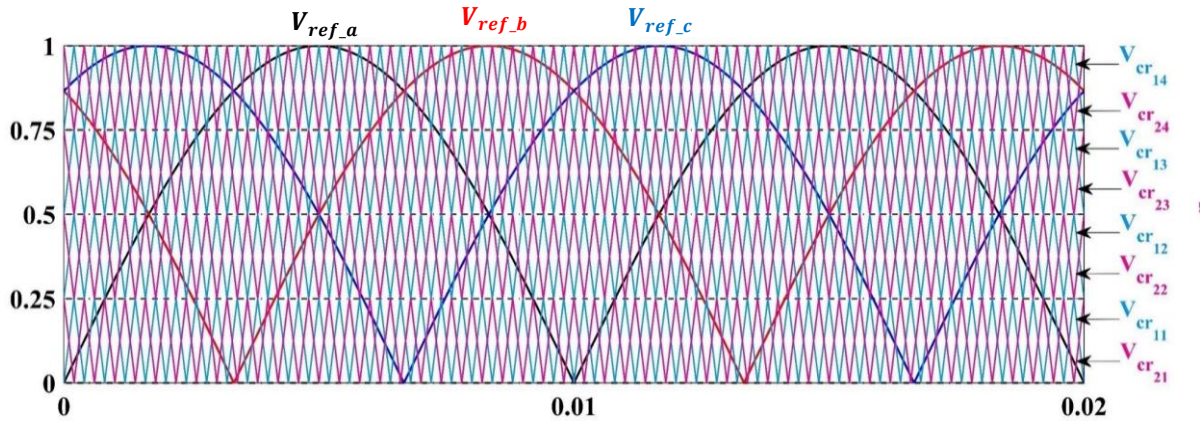


Figure 4. Hybrid-PWM for the proposed three-phase 17-level CSC-MLI

Theoretical Analysis of the Proposed CSC-MLI

Capacitance Design: The voltage rating of DC-link capacitors ($C_{11}, C_{12}, C_{21}, C_{22}$) and the floating capacitors ($C_{13}, C_{14}, C_{23}, C_{24}$) of each phase is equal to $V_{dc}/2$ and $V_{dc}/4$ respectively. The capacitance of DC-link capacitors is calculated as (Baksi, 2023):

$$C_{DC-link} = \frac{P_g}{4\pi\, f_g\, V_{dc}\, \Delta V_{dc}} \tag{2}$$

As the DC-link capacitors of each cell connected in series, So

$$C_{11} = C_{12} = C_{21} = C_{22} = 2C_{DC-link} \tag{3}$$

Where P_g represent the per-phase output power, $f_g$is the grid frequency and ΔV_{dc} represent the ripple voltage (5–0% of V_{dc}). The floating capacitance can be calculated as (Baksi, 2023):

$$C_F = \frac{I_{g,max}}{\Delta V_c \, f_{sw}} \tag{4}$$

As the floating capacitors of each cell connected in series, So

$$C_{13} = C_{14} = C_{23} = C_{24} = 2C_F \tag{5}$$

where $i_{g,max}$ is the maximum amplitude of per phase grid current and ΔV_c is allowable ripple voltage (2–5% of $\frac{V_{dc}}{4}$) in the floating capacitors.

Soft Charging Inductance Design: A charging inductor (L_{CH}) along with a freewheeling diode (D_f) is connected in series with the capacitor charging path to limit the inrush current. The inductor prevents sudden current changes and attenuates the inrush current, but it results in voltage spikes. Therefore, a diode is connected in parallel with the soft charge inductor to prevent this overvoltage issue in the inverter output voltage. This diode hinders overcharging of the capacitors and leads to steadying of the voltage of the capacitors. The value of the soft charging inductor can be calculated as (Jahan, 2018):

$$L_{CH} = \frac{1}{(2\pi f_g)^2 \alpha \, C_F} \tag{6}$$

Where α represents the number of ideal and identical cells.

Voltage and Current Stress of Switches: According to the switching state that is shown in Table 1, the maximum voltage stress across each switch of CSC-MLI is expressed as,

$$V_{S_{19}} = V_{S_{29}} = \frac{V_{dc}}{4} \tag{7}$$

$$V_{S_{11}} = V_{S_{12}} = V_{S_{21}} = V_{S_{22}} = \frac{V_{dc}}{2} \tag{8}$$

$$V_{S_{13}} = V_{S_{14}} = V_{S_{17}} = V_{S_{18}} = V_{S_{23}} = V_{S_{24}} = V_{S_{27}} = V_{S_{28}} = V_{dc} \tag{9}$$

$$V_{S_{15}} = V_{S_{16}} = V_{S_{25}} = V_{S_{26}} = 1.5\, V_{dc} \tag{10}$$

It is clear that $1.5\, V_{dc}$ is the maximum voltage stress that can occur across switches. By summing the voltage stress of each switch, the Total Standing Voltage (TSV) of the proposed CSC-MLI can be calculated:

$$TSV_{SW} = \sum_{ij=11}^{N_{SW}} V_{S_{ij}} \tag{11}$$

In the SC-MLIs, some switches carry additional current as a result of capacitor charging. In the suggested structure, the capacitor charging current (i_c) passes through the switches of the first basic cell S_{13}, S_{14}, S_{17} and S_{18}, as well as the switches of the second cell S_{23}, S_{24}, S_{27} and S_{28}. Consequently, it has high current stress as compared with the others that carry only the injected grid current (i_g). Each CSC-MLI switch's maximum current stress can be represented mathematically as follows:

$$i_{S_{11}} = i_{S_{12}} = i_{S_{15}} = i_{S_{16}} = i_{S_{19}} = i_{S_{21}} = i_{S_{22}} = i_{S_{25}} = i_{S_{26}} = i_{S_{29}} = i_g \tag{12}$$

$$i_{S_{13}} = i_{S_{14}} = i_{S_{17}} = i_{S_{18}} = i_{S_{23}} = i_{S_{24}} = i_{S_{27}} = i_{S_{28}} = (i_g + i_c) \tag{13}$$

Control Scheme of the Proposed System

A three-phase grid-tied 17-level CSC-MLI integrated with a multi-array PV system is implemented as illustrated in Fig. 5. The main controller objectives are to achieve optimum power transfer to the grid, operate the system under a variety of power factor (PF) conditions, and minimize the THD in the grid currents. In the proposed

configuration, the Voltage Oriented Control (VOC) grid-connected inverter loop is used to control the single DC-bus voltage (Mondol, 2023).

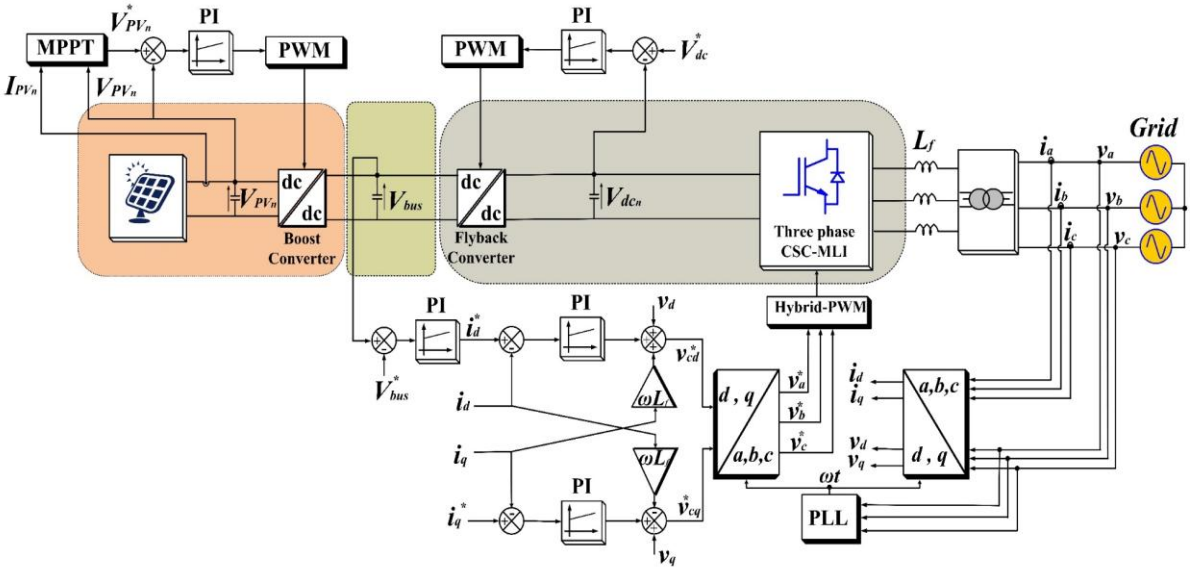


Figure 5. Control scheme of grid-tied 17-level CSC-MLI integrated with multi-array PV systems

The outer voltage loop and the inner current loops are the two parts of this control diagram. The voltage control loop is used to generate a reference d-axis current (i^*_d) by comparing the reference DC bus voltage V^*_{bus} with the measured V_{bus} , and it is responsible for controlling the active power. While the q-axis reference current will be adjustable and it is responsible for controlling the reactive power. The dq currents are controlled using PI controller and its outputs are added with the feedforward crossed compensation components (ωL_f) to produce the dq reference voltages. Which are converted into three-phase reference signals to be modulated by the Hybrid-PWM to generate gate pulses. Proper grid synchronization is essential for correctly aligning the dq frame with the grid voltage vector. So, a PLL has been used.

The Flyback converters control the DC-link voltage of each CSC-MLI cell to provide a fixed input DC-link voltage by changing the duty ratio of the flyback transistor using PWM. Finally, the multi-array boost converter with independent MPPT for each array uses a perturb and observe (P&O) MPPT technique due to its simplicity and performance.

Comparative Study

The proposed inverter is compared with some presented 17-level SC-MLIs in terms of the number of input DC supplies (N_{DC}) , switches (N_{SW}), diodes (N_{dio}), capacitors (N_{cap}), TSV, THD of the injected grid current, limiting the capacitor inrush current, grid-connected ability, and the per-phase output power. The findings of this comparison are detailed in Table 2.

Table 2. Comparison of a single-phase leg of the proposed inverter with recently introduced 17-level SC-MLI

Topology	N_{DC}	N_{SW}	N_{dio}	N_{Cap}	$TSV * (V_{DC})$	$\%\ THD\ i_a$	Per-Phase output power (W)	Limitation of capacitor spike current	Grid-connected
[6]	6	9	3	1	20	-	-	No	No
[13]	4	14	0	4	44	-	1000	No	No
[23]	1	14	4	4	82	-	522	Yes	No
[30]	2	14	2	4	40	-	3000	No	No
[31]	4	14	0	2	48	1.62	750	No	No
Proposed	2	18	4	8	16.5	0.5	4000	Yes	Yes

It is clear from the comparison table that the proposed inverter has a higher number of switches compared with the presented inverters which increase the complexity of the circuit, but its TSV is remarkably lower than other structures, where TSV is an essential factor in analyzing the feasibility of topology, as it is an indirect indicator of the switches' ratings and cost. While the structure in Ref. [6] has a suitable TSV, the main drawback is the have increased number of DC supplies. In contrast, the Ref. (Ali et al., 2022) required a single DC source but it suffered from high voltage stress across switches with the highest TSV. The topologies in Bana et al. (2019), Dhanamjayulu et al. (2021), Barzegarkhoo et al. (2017) and (Majhee et al., 2019) the disadvantage of employing switches with a high current rating because of the high inrush current during the capacitor charging mode. Both Ali et al. (2022) proposed inverter and restrict the capacitive charging current spike, making them suitable for high-power applications. Compared to the presented inverter, the proposed inverter is the superior one with a high-quality injected grid current of lower THD and a very high inverter output power.

Results and Discussion

The proposed three-phase 17-level CSC-MLI and control scheme are simulated using MATLAB/Simulink platform. A three-phase 17-level CSC-MLI connected to a 380 V/ 50 Hz grid through a simple filter $L_f = 1\ mH$ is considered for simulation results. The stage of injecting PV power consists of three PV arrays with independent boost converters simulated by linking it to a single DC bus bar. On the other side, two Flyback converters for each phase have been implemented for supplying two basic cells with a DC-link voltage of $V_{dc} = 170$ V. The specifications of the PV array and the proposed configuration are listed in Tables 3 and 4, respectively.

Table 3. Specifications of the PV panel for each PV array

Parameters	Value
No. of series-connected panels per string (N_s)	4
No. of parallel string (N_p)	4
Maximum power of each panel (P_{mpp})	260 W
Maximum current at MPP (I_{mpp})	8.6A
Maximum voltage at MPP (V_{mpp})	30.25 V
Maximum power of each array (P_{PV})	4160 W
Total generated PV power of the three arrays (P_{PV_T})	12.48 KW

Table 4. Specifications for testing the proposed CSC-MLI

Parameters	Value	Unit
V_{bus}	200	V
V_{dc_1}, V_{dc_2}	170	V
V_g (L-L)	380 (rms)	V
L_f	1	mH
C_{bus}	6000	µF
$C_{dc-link}$	3250	µF
C_F	5000	µF
f_{sw}	2.5	kHz
f_g	50	Hz
L_{CH}	0.5	mH

Firstly, to illustrate how well the grid-connected inverter control system performs dynamically, the system's behavior is examined under an irradiation step change from 700 to 1000 W/m^2 at t = 0.45s as shown in Fig. 6 (a). Fig. 6 (b) illustrates that due to the increase in generated power, the DC-bus voltage V_{bus} experiences a slight increase before controlled back to its reference level by the CSC-MLI outer loop control. Fig. 6 (c) illustrates the per-phase DC-link voltages (V_{dc_1} , V_{dc_2}) which proves the effectiveness of the Flyback converter in maintaining a constant input DC voltage despite the changes of V_{bus}. It is clear that the 17-level inverter output voltage (V_C) are not affected by the swell in the DC bus voltage, as the Flyback converter regulates the input DC-link voltages as shown in Fig. 6 (d). As illustrated in Fig. 6(e), the control loop raises the d-axis current in response to increased power generation. As a result, increase the injected grid currents. A scaled grid voltage of phase-a has been included to demonstrate the appropriate grid synchronization that achieved by the PLL.

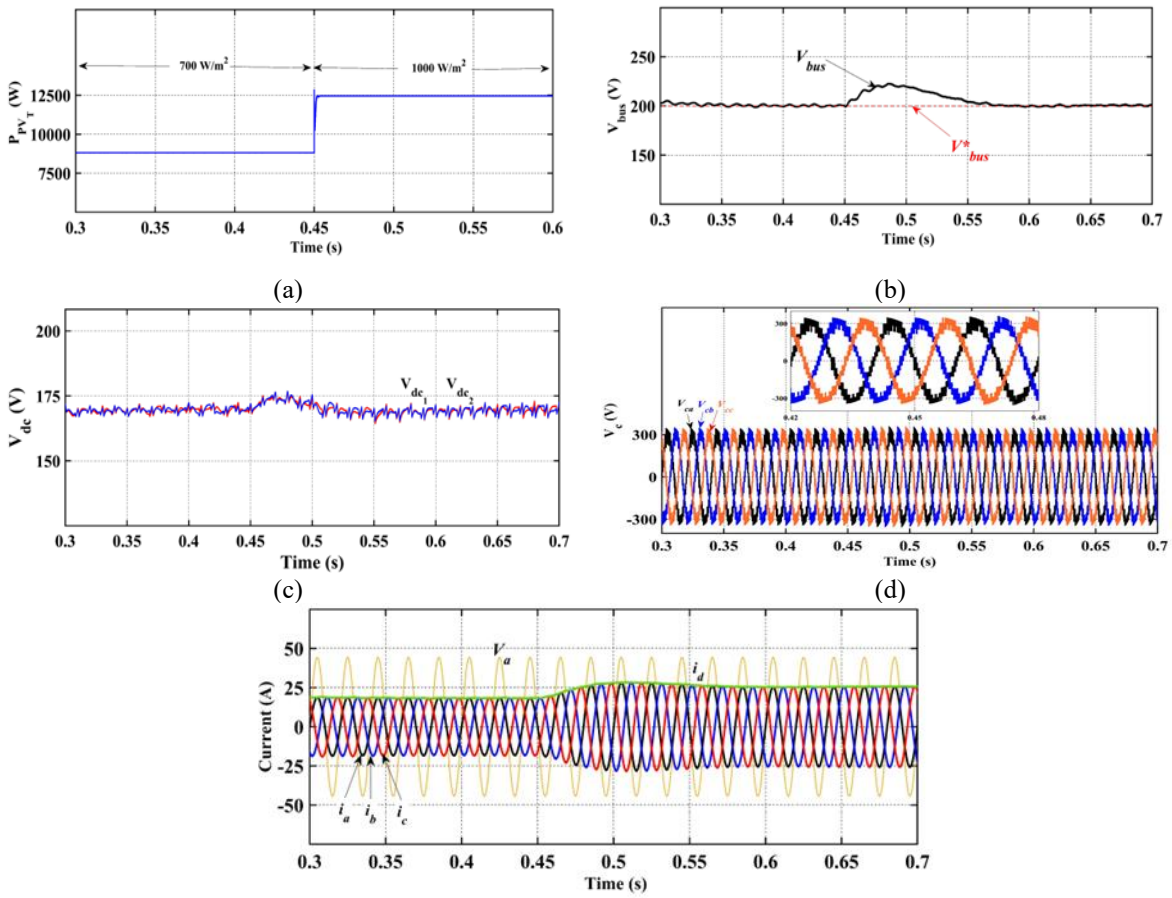
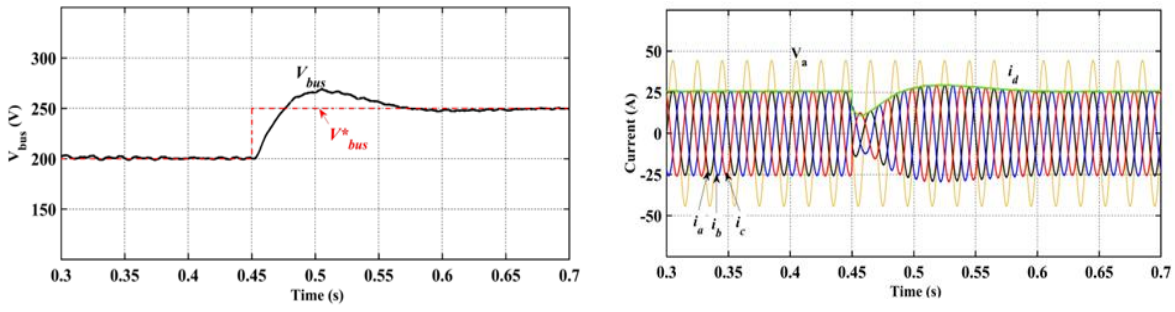
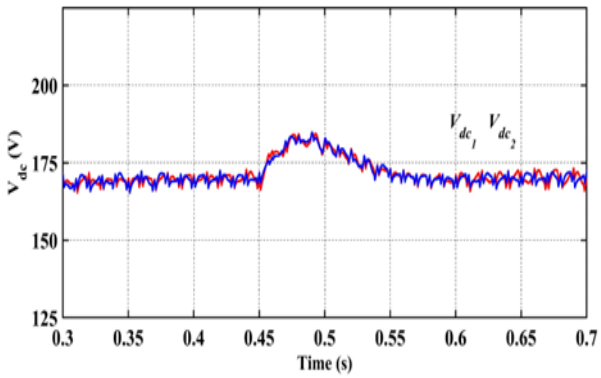


Figure 6. Performance of the control scheme under power generated step: a) PV power, b) dc-bus voltage with reference, c) DC-link voltages, d)17-level three-phase inverter output voltages, e) grid currents and d-axis current with scaled phase a voltage.

Next, a step change in the DC bus reference voltage is increased at t = 0.45s from 200 to 250V, as can be observed in Fig. 7 (a). To accomplish this voltage rise, the grid currents are slightly reduced and then returned to their value to use the incoming PV power to charge the DC bus capacitor as shown in Fig. 7 (b). Note however from Fig. 7 (c), the per-phase CSC-MLI DC-link voltages are maintained at around 170 V, since the Flyback converter adjusts its duty cycle accordingly. The Flyback converter isolates dynamic fluctuations in the PV system, keeping the DC-link voltages of the cells constant. This leads to improved overall performance and achieving a better grid current regulation.

After verifying the proposed inverter control scheme's performance, the proposed configuration is tested under different scenarios to demonstrate the topology's actual performance as follows:



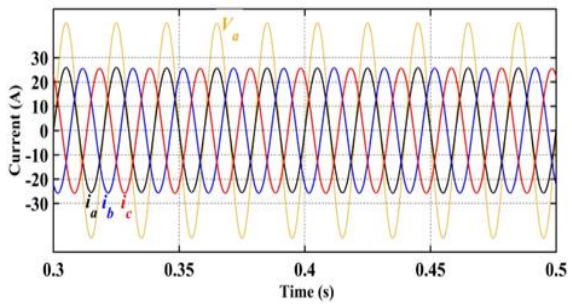


(c)

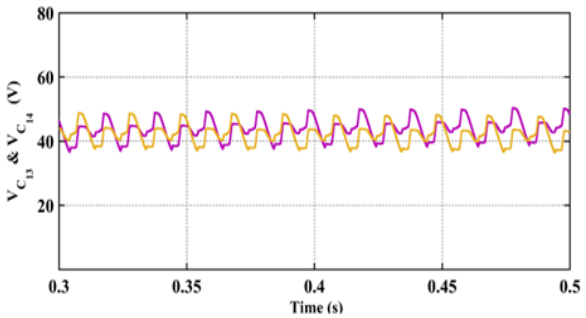
Figure. 7. Performance of the control scheme under step change in DC bus reference voltage: a) dc-bus voltage with reference, b) grid currents and d-axis current with scaled phase a grid voltage, c) DC-link voltages

1- Testing Under Steady-State Conditions: The performance of the proposed three-phase grid-tied PV system utilizing the suggested inverter under steady-state conditions is illustrated in Fig. 8. Simulation results under steady-state conditions, showing injected three-phase currents, floating capacitor voltages, and charging currents. In this condition, solar irradiation is held constant at 1000 W/m^2, and the power factor is maintained at unity. Three PV arrays with independent boost converters have been used with a maximum generated power for each array equal to 4160 W to generate a total PV power of 12.48 kW. After meeting the system losses, the total injected power to the grid (P_g) is 12 KW. The three-phase injected currents to the grid are depicted in Fig. 8(a). The peak magnitude of V_a and i_a are 311 V and 25.75 A respectively. Owing to the unity power factor operation, both V_a and i_a are in phase. Fig. 8(b) has shown the voltage across floating capacitors. It can be seen they are always having balanced magnitude equal to ($V_{dc}/4$), which verifying the capability of self-balancing capacitor voltages.

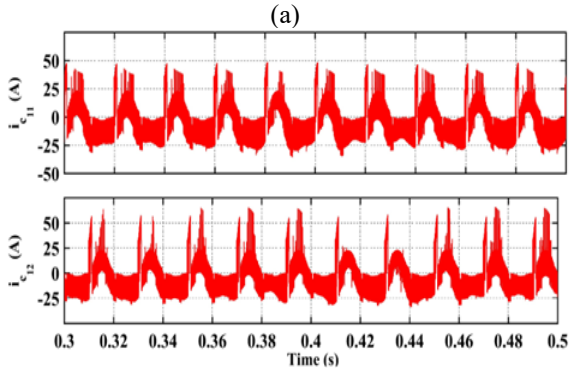
As mentioned, one of the most important features of the proposed inverter is the ability to limit the capacitor inrush current during the capacitor charging mode, by employing a soft charging method. Fig. 8(c) and Fig. 8(d) indicate the per-phase capacitor charging current waveform of DC-link capacitors and floating capacitors of the first basic cell, as both cells are identical. Based on Fig. 8(c), the maximum value of the capacitor charging current spike of C_{11} and C_{12} are 47 A and 60 A, respectively. While of C_{13} and C_{14} it will be 65 A as shown in Fig. 8 (d). Which proves the good performance of the soft charging method.



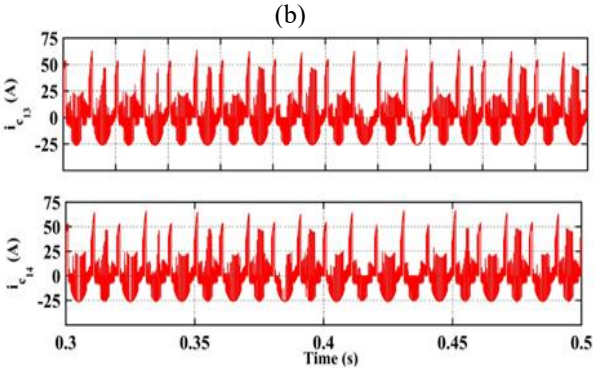
(a)



(b)



(c)



(d)

Figure 8. Simulation results under Steady-State conditions, a) injected three-phase currents, b) Per-cell floating capacitors voltage, c) DC-link capacitors current, and d) floating capacitors current.

2- Testing Under Varying Irradiance: A step change in irradiance from 1000 W/m^2 to 500 W/m^2 is applied at t= 0.7 s, and then it stepped up to 1000 W/m^2 at t= 1.4 s and the power factor was kept in unity during this simulation by setting i^*_q= 0. The waveform of the total PV power P_{PV_T} is shown in Fig. 9(a). The magnitude of P_{PV_T} is 12.48 kW and 6.314 kW corresponding to 1000 W/m^2 and 500 W/m^2 irradiance, respectively. After achieving system losses, the injected power will be 12 kW and 6.2 kW corresponds to 1000 W/m^2 and 500 W/m^2 irradiance, respectively. Fig. 9 (b) illustrates that the injected three-phase grid currents i_{abc} decreases as solar irradiation decreases. The peak magnitude of i_{abc} reduced from 25.75 A to 13.3 A when irradiance decreased from 1000 W/m^2 to 500 W/m^2 . Fig. 9 (c) illustrates the THD content of the i_a measured as 0.5 % and 0.78 % corresponding to 1000 W/m^2 and 500 W/m^2 irradiance, respectively, which complies with IEEE standards.

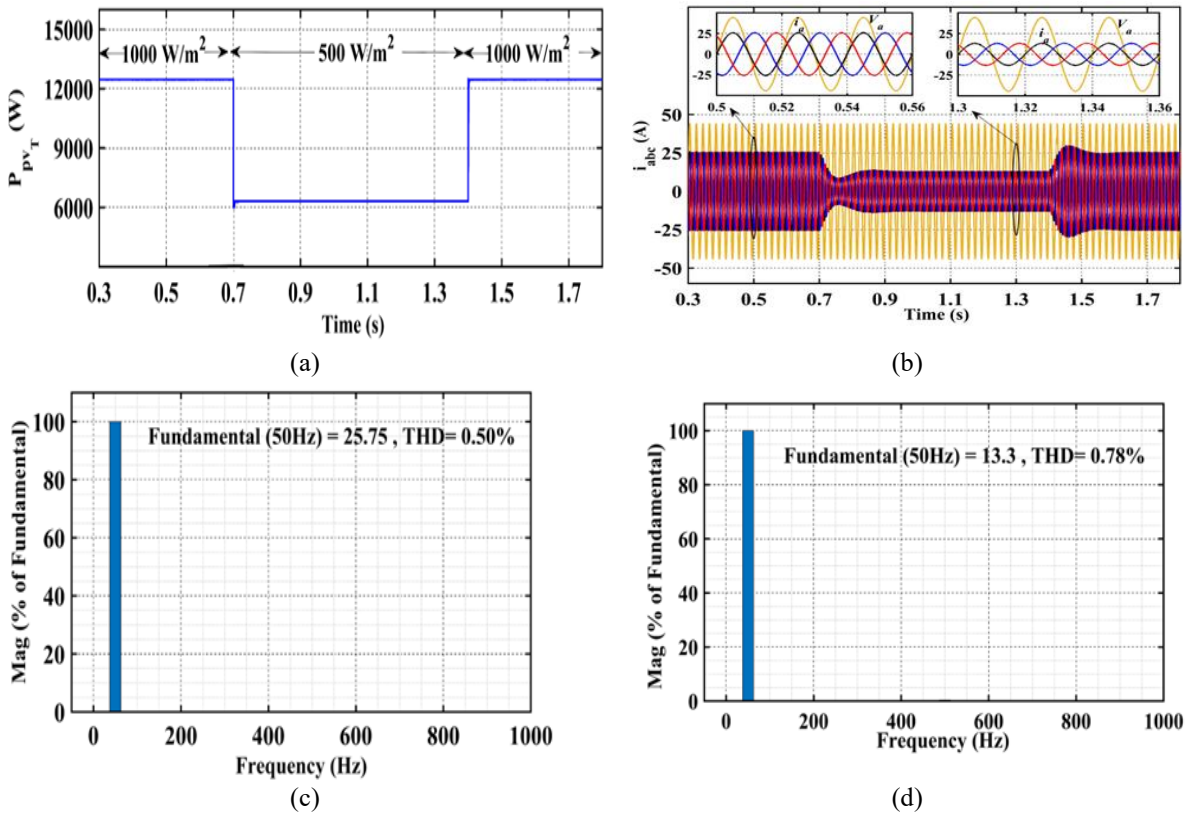


Figure 9. Simulation results under varying irradiance conditions, a) generated PV power, b) injected three-phase currents, c) THD content of i_a at 1000 W/m^2 , and d) THD content of i_a at 500 W/m^2

3-Testing Under Various Power Factor Conditions: To assess the dynamic performance of the proposed grid-connected system, a step change in the power factor (PF) was applied from unity PF to leading PF. Throughout the test, the irradiance level was kept constant at 1000 W/m^2. Initially, the system operated at unity PF. Then, at t = 0.7 s, the power factor was abruptly adjusted to 0.85 leading PF. Later, at t = 1.4 s, it was changed back to unity PF. It is observed that from Fig. 10(a), the inverter receives zero reactive power from the grid for UPF and 7.43 kVAR for 0.85 leading power factor which it the maximum reactive power that can be absorbed by the proposed inverter. While the injected real power P_g remains constant to 12 kW despite the changing of PF. From Fig. 10(b), it is noticed that the magnitude i_a increased from 25.75 A to 30.2 A and it is lead V_a by 31.78 ˚ for 0.85 leading PF. The quality of the grid current remains high with a THD of 0.76% as observed in Fig. 10 (c).

The proposed configuration was then tested under a step change of the power factor from unity PF to lagging PF. Initially, the system operated at Unity PF. Then, at t = 0.7 s, the power factor was abruptly adjusted to 0.85 lagging PF. Later, at t = 1.4 s, it was changed back to unity PF. From Fig. 11(a), we can observe that the reactive power injected into the grid is zero under unity power factor (UPF) condition but increases to 7.43 kVAR when operating at a 0.85 lagging power factor, which it the maximum reactive power that can be injected into the grid by the proposed inverter. While the injected real power P_g remains constant to 12 kW. Fig. 11(b) shows that the magnitude of i_a increased from 25.75 A to 30.2 A and it is lag V_a by 31.78 ˚ during 0.85 lagging PF. The quality of the grid current remains high with a THD of 0.56% as can be seen in Fig. 11 (c).

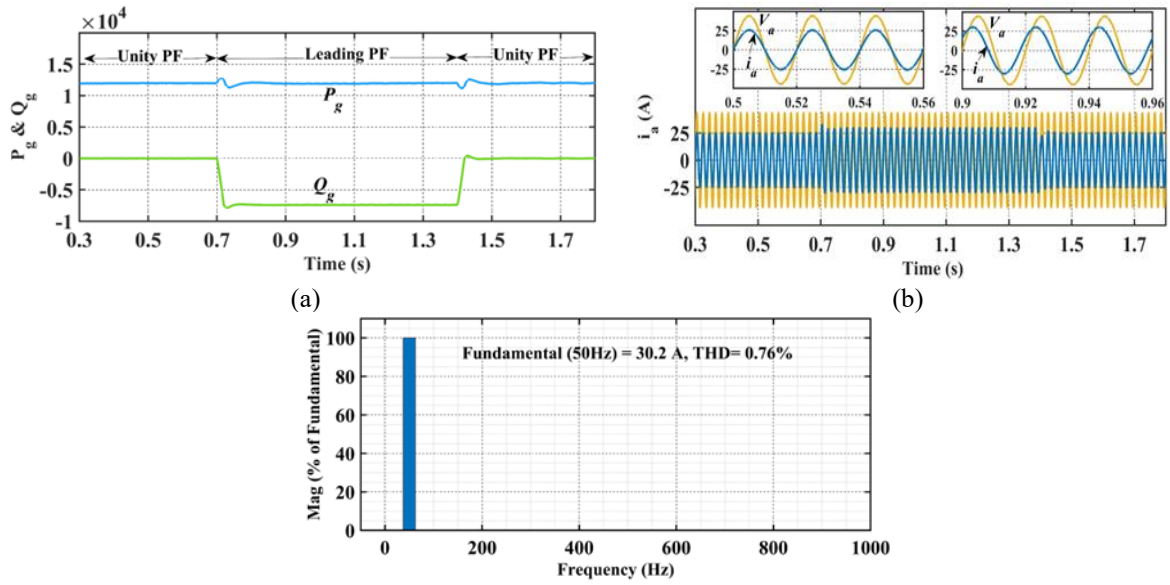


Figure 10. Simulation results under varying power factors from unity PF to leading PF. a) injected active and reactive power, b) injected grid current of i_a with scaled V_a, c) THD content of i_a at leading PF.

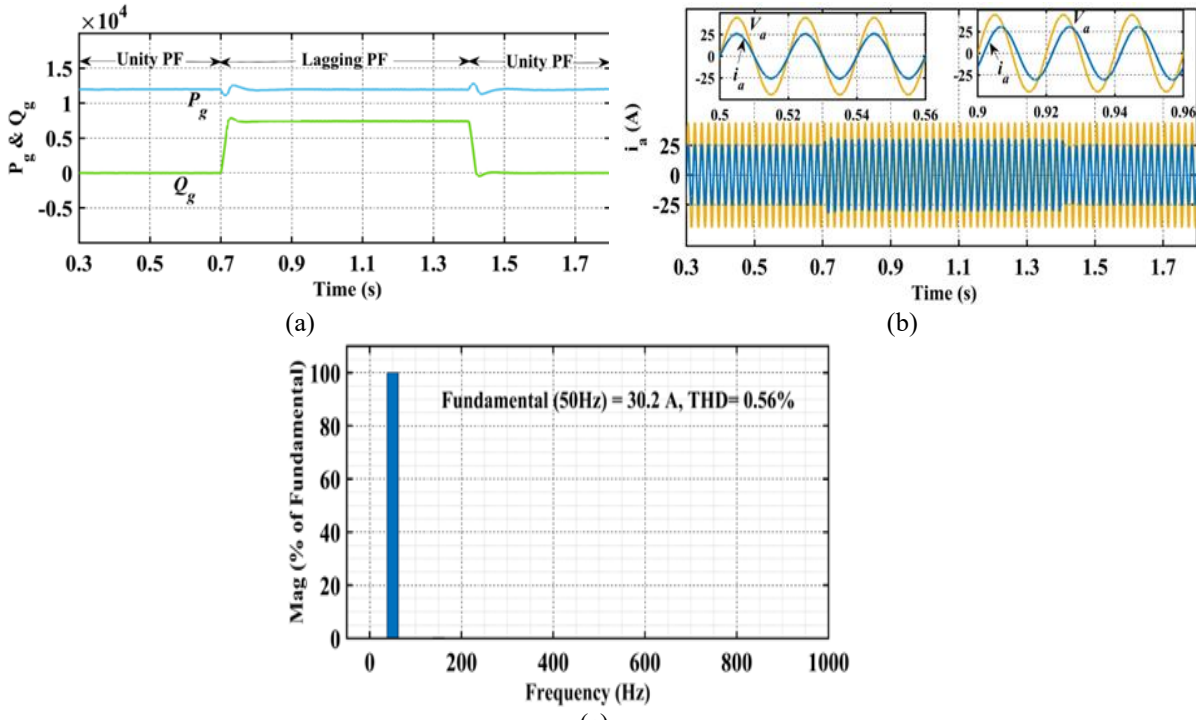


Figure 11. Simulation results under varying power factors from unity PF to lagging PF. a) injected active and reactive power, b) injected grid current of i_a with scaled V_a, c) THD content of i_a at lagging PF.

Therefore, from the previous tests, it is concluded that the proposed photovoltaic grid system has good steady-state and dynamic performance and the performance of the proposed inverter doesn't affect despite changing the PF.

Conclusion

This paper proposes a grid-connected three-phase 17-level cascaded switched-capacitor multilevel inverter (CSC-MLI) integrated with multi-array PV systems through a single DC bus bar. Each phase of the proposed inverter employs 2 isolated DC sources with twelve unidirectional switches, six bi-directional switches, four diodes, four

DC-link capacitors and four floating capacitors in order to generate seventeen different output voltage levels with a 2 times voltage gain. Both polarities are obtainable at the output without using H-bridge, lower voltage rating of switches, self-voltage balancing of the capacitor, limiting the capacitor inrush current, and reduced TSV have been the main features of the proposed topology. In addition, the amount of the reactive power injected into the grid can be controlled by the inverter. Under a variety of test conditions, the simulation results confirm the system's reliable performance and compliance with IEEE standards for THD content in the injected grid current.

Scientific Ethics Declaration

* The authors declare that the scientific ethical and legal responsibility of this article published in EPSTEM journal belongs to the authors.

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Conflict of Interest

* The authors declare that they have no conflicts of interest.

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